WHAT IS CLAIMED IS:

1. A thin film transistor array panel comprising:

first and second gate members connected to each other;

a gate insulating layer formed on the first and the second gate members;

first and second semiconductor members formed on the gate insulating layer opposite the first and the second gate members, respectively;

first and second source members connected to each other and located near the first and the second semiconductor members, respectively;

first and second drain members located near the first and the second semiconductor members, respectively, and located opposite the first and the second source members with respect to the first and the second gate members, respectively; and

a pixel electrode connected to the first and the second drain members,

wherein the first gate member, the first semiconductor member, the first source member, and the first drain members form a first thin film transistor, and the second gate member, the second semiconductor member, the second source member, and the second drain members form a second thin film transistor.

2. The thin film transistor array panel of claim 1, wherein the first thin film transistor and the second thin film transistor are symmetrically aligned.

3. The thin film transistor array panel of claim 2, wherein the alignment of the first and the second thin film transistors are symmetrical with respect to a predetermined line.

4. The thin film transistor array panel of claim 3, wherein the predetermined line includes a boundary line between shots in light exposure.

5. The thin film transistor array panel of claim 4, further comprising a third thin film transistor different from the first and the second thin film transistors.

6. The thin film transistor array panel of claim 1, wherein the alignment of the first and the second thin film transistors are located opposite each other with respect to a boundary line between shots in light exposure.

7. The thin film transistor array panel of claim 1, wherein channels of the first and the second thin film transistors have curved shapes.

8. The thin film transistor array panel of claim 7, wherein channels of the first and the second thin film transistors have U or C shapes.

9. The thin film transistor array panel of claim 1, wherein the first and the second semiconductor members have substantially the same planar shapes as the first and the second source and drain members except for channel portions of the first and the second thin film transistors.

10. A method of manufacturing a thin film transistor array panel, the method comprising:

forming a pair of first and second gate members;

forming a gate insulating layer on the first and the second gate members;

forming a pair of first and second semiconductor members on the gate insulating layer;

forming a pair of first and second source members and a pair of first and second drain members; and

forming a pixel electrode connected to the first and the second drain members,

wherein at least one pair of the first and the second gate members, the first and the second semiconductor members, the first and the second source members, and the first and the second drain members are formed using a divisional light exposure, and a boundary line between shots in the divisional light exposure is located between the first gate member and the second gate member, between the first semiconductor member and the second semiconductor member, between the first source member and the second source member, or between the first drain member and the second drain member.

11. The method of claim 10, wherein the at least one pair has a shape symmetrical with respect to the boundary line.